REMARKS

This paper is responsive to the Non-Final Office Action dated December 8, 2005. Claims 1-44 were examined.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 3, 13, 21, and 32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chappell et al. (U.S. Patent No. 4,845,669). Applicant respectfully traverses this rejection in part.

Regarding claim 1, Applicant respectfully submits that even though Chappell describes an architecture "for providing equally fast access to stored data in two or more dimensions", it is not believed that Chappell describes or even suggests an *integrated circuit* having a *three-dimensional memory array*. For example, Chappell refers to U.S. Patent No. 4,447,891 to Kadota as describing:

> an array of bit storage cells (memory cells) with two complementary vertical word lines (address lines) and two complementary horizontal bit lines (data lines). The two complementary horizontal bit lines (data lines) are connected through gate elements to complementary input-output nodes, while the gate elements are controlled by the vertical word lines (address lines). The word lines being parallel and the bit lines being parallel provides only single dimension accessing of stored data.

(Column 1, lines 24-33) In addition, Chappell refers to U.S. Patent No. 4,368,523 to Kawate as describing:

> a matrix of memory cells wherein the address buses (word lines) are connected to the rows of the memory cells in the matrix while the data buses (bit lines) are connected to the columns of the memory cells. The address buses run parallel to each other in the horizontal direction while the data buses run parallel to each other in the vertical direction, thereby providing access to data in only one dimension.

(Column 1, lines 45-53) In both such references, the memory arrays are unquestionably two-dimensional memory arrays (e.g., horizontal word lines and vertical bit lines), yet the access is described as being *single dimensional*.

Similarly, Chappell's use of *multi*-dimensional access does not necessarily imply a memory array that is three-dimensional, or different at all. For example, Chappell states that:

> U.S. Pat. No. 3,800,289 to Batcher features multidimensional access capability achieved with address level manipulation. The memory array has a single address selection input and a single output path. This patent does not teach orthogonal address capability implemented at the cell/array level.

(Column 2, lines 45-50). This memory array is unquestionably a traditional two-dimensional memory array, yet achieves multi-dimensional access capability.

Applicant believes that the multi-dimensional access that Chappell teaches is achieved within a single array by an orthogonal address capability implemented within a memory array. For example, as shown in Fig. 1-Fig. 5, a plurality of Dimension I word lines traverses the array orthogonal to a plurality of Dimension II word lines. Each plurality of word lines has a corresponding orthogonal plurality of bit lines.

Applicant also believes that Chappell does not teach or suggest his methods in the context of a three-dimensional memory array having more than one plane of memory cells. For example, one of the stated objects of Chappell's invention is "to provide the above single-ended reading in multi dimensions using only one word line, one bit line and one access device per bit per dimension." (Column 2, lines 62-65). There is no suggestion of requiring *or even making use of* additional memory cells in his array to achieve each additional dimension of access. Instead, he modifies a given memory cell for each additional dimension of access to that memory cell.

Moreover, in describing the multi-array TMA device shown in Fig. 5 (having four separate TMA cell arrays (three of which are labeled 50, while the fourth is labeled 20), Chappell teaches that:

> An alternate embodiment of the MTMA device could use the *multiple arrays* to provide rapid accessing of data in *more than two-dimensions*. Dedicated data-in buses along with dedicated decoders to each array could provide a shifting of data written-into one array relative to the same data written into another array. *If n arrays are thus used, then a read access*

> *through the TMA arrays could provide any one or all of 2n data-units from 2n dimensions simultaneously.*

(Column 8, lines 21-29) Thus, the described multi-dimensional access is accomplished using multiple laterally-spaced cell arrays, each apparently providing but two dimensions of access, as described above. Nowhere does Chappell suggest any embodiments using a *three-dimensional memory array* to provide his *multi-dimensional access* of one or more memory arrays.

One of the implications of Chappell's orthogonal sets of word lines is that the first set of word lines exits the memory array on one side of the array (e.g., in Fig. 5, the Dimension I word lines WLI exiting to the left side of the memory array 50) while the second set of word lines exits the memory array on an adjacent side of the memory array (e.g., the Dimension II word lines WLII exiting to the top of the memory array 50). The two sets of word lines do not exit the memory array on opposite sides of the memory array. Similarly, the two sets of bit lines (BLI and BLII) do not exit on opposite sides of the memory array, as they exit the array on adjacent sides as well.

In light of these distinctions, Claim 1 has been amended to now recite:

> An integrated circuit having two respective decode/selection circuits respectively located along opposite edges of a three-dimensional memory array for selecting wordlines ~~or bitlines~~ which respectively exit the memory array along said opposite edges or for selecting bitlines which respectively exit the memory array along said opposite edges.

Applicant respectfully submits that the claim clearly recites a structure which is not taught or suggested by Chappell, and requests that the rejection be withdrawn as to this claim.

Regarding claim 13, Applicant respectfully submits that Chappell does not teach or suggest all the limitations of the claim. Specifically Chappell does not teach or suggest an integrated circuit including a three-dimensional memory array having at least two planes of memory cells formed above a substrate. The cited portions relied upon by the Examiner include Fig. 4 as allegedly showing two planes of memory cells formed above a substrate. Applicant respectfully submits that Fig. 4 depicts a single plane of memory cells and illustrates the transposition of the data-unit that results from switching the dimension bit while keeping the

word and bit addresses fixed. (Column 6, lines 18-21) The memory cells within a single two-dimensional plane of memory cells are accessed either by rows or by columns depending upon the dimension address:

> In contrast to the conventional memory architecture, an additional address-- the "dimension address"-- (received through input port 35) defines the dimension from which the data-unit is to be selected or, possibly, to which it is to be written. FIG. 4 illustrates the transposition of the data-unit that results from switching the dimension bit while keeping the word and bit addresses fixed. Suppose, for example, a particular address plus a "1" dimension bit state results in the third data-unit (42) of dimension I being read, which is in the third row of the FIG. 4 data block. Then, switching the dimension bit to the "0" state without changing the word or bit address results in the third data-unit (44) of dimension II being read, which is the third column of the FIG. 4 data block. Accomplishing the same transposition in the case of a conventional memory architecture, would require many cycles of the TMA device; typically, the number of cycles required would be equal to the width of the data-unit (8 in FIG. 4).

(Column 6, lines 14-32) Applicant finds no suggestion of more than one memory plane in this teaching. Nonetheless, Applicant has amended the claim to recite a similar limitation as was included in claim 1. Claim 13 now recites:

> An integrated circuit comprising:
> a three-dimensional memory array having at least two planes of memory cells formed above a substrate;
> a first decode/selection circuit having outputs associated with wordlines or bitlines which exit on one edge of the memory array; and
> a second decode/selection circuit having outputs associated with wordlines or bitlines which exit on another edge opposite the one edge of the memory array;
> wherein the outputs of both the first and second decode/selection circuits are associated with wordlines, or the outputs of both the first and second decode/selection circuits are associated with bitlines.

Applicant respectfully submits that the claim clearly recites a structure which is not taught or suggested by Chappell, and requests that the rejection be withdrawn as to this claim.

Regarding claim 21, Applicant submits that this claim is allowable at least for its dependence from claim 15 (which was objected to). Moreover, it is also believed allowable for its dependence from allowable claim 13, particularly as amended.

The remaining presently-rejected dependent claims 3 and 32 are also believed allowable at least for their dependence from an allowable independent claim. Applicant thus believes this rejection has been overcome and respectfully requests its withdrawal.

Allowable Subject Matter

Claims 2, 4-12, 14-20, 22-31, and 33-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 10 has been so rewritten. In light of the believed allowability of the independent claims, the remaining claims remain without amendment.

Summary

Claims 1-44 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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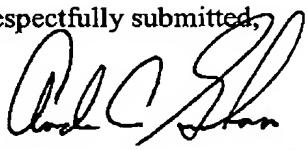
Respectfully submitted,



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